AMENDMENT TO THE CLAIMS

This listing of claims will replace all prior versions of claims in the application.

Listing of Claims:

1-12. (canceled)

13. (currently amended) A ~~dense~~ memory cell comprising:

a plurality of access transistors~~, each having a gate tied to a wordline input, a first one of the access transistors having a drain and source coupled between a bit line and an output node~~ having their gates coupled to a wordline and when activated by an input signal on the wordline, the access transistors to allow coupling of a bit line to a storage node or to allow coupling of a complement bit line to a complement storage node;

a plurality of storage transistors, in which a first ~~one having a drain and source~~ storage transistor is coupled between the ~~output line~~ storage node and a power ~~signal~~ supply node and ~~a~~ its gate coupled to ~~an output bar node, the second one having a drain and source~~ the complement storage node, and a second storage transistor coupled between the ~~output bar~~ complement storage node and the power ~~rail,~~ supply node and ~~a~~ its gate coupled to the ~~output~~ storage node; and

a control circuit ~~generating~~ coupled to monitor voltage on the storage node, compare the monitored voltage on the storage node with a reference voltage and in response, to generate a tracking voltage coupled to the wordline~~, the track voltage for adjusting the voltage on the wordline to cause~~ to adjust leakage current through the ~~two~~ access transistors to exceed leakage through the plurality of storage transistors.

14. (currently amended) The memory cell of claim 13 wherein the ~~tracking voltage is a function of a~~ reference voltage ~~determined to provide a leakage through the access transistors that exceeds the leakage through the storage devices~~ is programmable.

15. (currently amended) The memory cell of claim ~~14~~ 13 wherein the tracking voltage is to be maintained substantially constant ~~by a differential amplifier~~.

16. (currently amended) The memory cell of claim 15 wherein the tracking voltage is buffered to substantially reduce disturbances ~~to VREF resulting from switching states on the wordline~~ caused by switching of the input signal on the wordline.

17. (currently amended) The memory cell of claim 15 ~~wherein the tracking voltage is generated by a reference circuit, the reference circuit comprising:~~ further comprising a plurality of partial memory cells, each partial memory cell ~~comprising~~ having at least one access transistor and at least one storage transistor ~~configured~~ to operate as a dummy cell, ~~in a worst case leakage condition; and a differential amplifier having a voltage reference input and a second input coupled to an output node of each of the partial memory cells, the output of the differential amplifier being the tracking voltage~~ and the control circuit to monitor a dummy storage node of the dummy cell to compare to the reference voltage to generate the tracking voltage on the wordline.

18-19. (canceled)

20. (currently amended) A method ~~of maintaining~~ to maintain a ~~preferred~~ leakage current ratio between access and storage devices in a memory cell~~, said method~~ comprising:

establishing a reference voltage that ~~is equal~~ corresponds to an ~~desired~~ output voltage of the memory cell;

generating a tracking ~~signal required to force~~ voltage in response to comparing the reference voltage ~~onto~~ with an output voltage of a dummy ~~circuit~~ cell; and

coupling the tracking ~~signal~~ voltage to a ~~point~~ location in the memory cell ~~wherein a leakage current is generated in each of the access and storage devices and further wherein the~~ to control leakage current in the access devices ~~is~~ to be greater than ~~the~~ leakage current in the storage ~~devices~~ device.

21. (currently amended) The method of claim 20 further including ~~varying the~~ using the tracking voltage to vary well to substrate bias voltage of the storage ~~devices~~ device to ~~decrease~~ control the leakage current through the storage ~~devices~~ device.

22. (currently amended) The method of claim 20 ~~wherein the control signal biases the supply rail voltage to which the storage devices are directly coupled to decrease the amount of~~ further including using the tracking voltage to vary bias on a node coupled to a supply rail to control the leakage current through the storage ~~devices~~ device.

23. (currently amended) The method of claim 20 ~~wherein a differential amplifier detects when the output state of a plurality of dummy cells have fallen below a~~

~~predetermined reference voltage~~ further including using the tracking voltage to adjust voltage on a wordline of the memory cell to vary gate bias of the access device to adjust the leakage current through the access device.

24. (currently amended) The method of claim 23 ~~wherein the differential amplifier generates the control signal at a level required to restore the output state to at or near the reference voltage~~ further including buffering the tracking voltage.

25. (currently amended) A ~~dense~~ memory cell comprising:

a plurality of access transistors~~, each having a gate tied to a well bias input, a first one of the access transistors having a drain and source coupled between a bit line and an output node~~ having their gates coupled to a wordline and when activated by an input signal on the wordline, the access transistors to allow coupling of a bit line to a storage node or to allow coupling of a complement bit line to a complement storage node;

a plurality of storage transistors, in which a first ~~one having a drain and source~~ storage transistor is coupled between the ~~output line~~ storage node and a power ~~signal~~ supply node and ~~a~~ its gate coupled to ~~an output bar node, and a second one having a drain and source~~ the complement storage node, and a second storage transistor coupled between the ~~output bar~~ complement storage node and the power ~~signal,~~ supply node and ~~a~~ its gate coupled to the ~~output~~ storage node; and

a control circuit ~~generating~~ to generate a tracking voltage that corresponds to a voltage on the storage node and to couple the tracking voltage to a substrate well of the first and second storage transistors to provide a well-substrate bias for the storage

transistors ~~coupled to the well bias, the track voltage for adjusting the voltage on the well bias during an idle state~~ to ensure that leakage current through the two ~~access~~ storage transistors ~~exceeds the~~ does not exceed leakage current through the two ~~storage~~ access transistors ~~where the output node to which it is coupled is at VDD~~.

26. (currently amended) The memory cell of claim 25 further comprising ~~a tracking circuit that comprises a number of half configured~~ a plurality of partial dummy memory cells that are placed in a state which mimics ~~the~~ a stored state ~~in a normal memory cell that would degrade during the idle state~~ of the storage transistors and in which stored state voltage from the dummy memory cells are to be used to generate the tracking voltage.

27. (currently amended) The memory cell of Claim 26 wherein the tracking voltage is a function of the stored state voltage from the dummy cells and a reference voltage ~~determined to provide a leakage through the storage transistors that is less than the leakage through the access devices~~.

28. (new) A memory cell comprising:

a plurality of access transistors having their gates coupled to a wordline and when activated by an input signal on the wordline, the access transistors to allow coupling of a bit line to a storage node or to allow coupling of a complement bit line to a complement storage node;

a plurality of storage transistors, in which a first storage transistor is coupled between the storage node and a power supply node and its gate coupled to the complement storage node, and a second storage transistor coupled between the complement storage node and the power supply node and its gate coupled to the storage node; and

a control circuit to generate a tracking voltage that corresponds to a voltage on the storage node and to couple the tracking voltage to a power supply node of the first and second storage transistors to provide a bias for the storage transistors to ensure that leakage current through the two storage transistors does not exceed leakage current through the two access transistors.

29. (new) The memory cell of claim 28 further comprising a plurality of partial dummy memory cells that are placed in a state which mimics a stored state of the storage transistors and in which stored state voltage from the dummy memory cells are to be used to generate the tracking voltage.

30. (new) The memory cell of Claim 29 wherein the tracking voltage is a function of the stored state voltage from the dummy cells and a reference voltage.